

**TESEDA’S SCAN WORKBENCH™**

**Teseda’s Scan WorkBench™** integrates Teseda’s award-winning DFT-aware, interactive scan fail debug environment into the IG-XL environment. **Scan WorkBench** fully exploits the power of a company’s DFT investment, enabling Design, Test, Manufacturing and FA teams to work together to reduce time to production, accelerate yield learning, and maximize profits.

(insert screen shot of Scan workbench for IG-XL here)

**Reduce Scan Debug Time by Up to 90%**

**Scan WorkBench** leverages the power of utilizing existing DFT structures designed into your silicon. Since the **Scan WorkBench** toolset automatically comprehends the DFT-Embedded design hierarchy of the device, scan-detected failures can be mapped to specific scan chains, scan cells and design blocks without the need for tedious deciphering of pin and cycle failure information. The DFT-aware environment of **Scan WorkBench** adds efficient debugging of common scan-detected device failures such as broken scan chains and scan-related timing violations, to IG-XL. Failures captured can be exported to be analyzed by scan fault diagnosis and analysis tools such as Mentor Graphics Yield Assist™, Synopsys TetraMAX™ and **Teseda’s Diagnostic Manager NetXY™.**

***Benefits of Scan WorkBench***

. Reduces silicon debug time to days instead of weeks

. Speeds diagnosis of yield-limiting defects

. Adds powerful, interactive DFT-aware scan debug capabilities to all major Teradyne ATE platforms

. Fully integrated into the IG-XL environment – minimal training needed

. Exports to EDA diagnosis and analysis tools such as Teseda’s **Diagnostic Managaer NetXY**

. Debug either online or offline from the tester

. Compatible with industry standards (IEEE 1450-1999 (STIL) and STDF V4 2007 (Data Log Format))

**Available on the Industry’s Most Popular ATE Systems**

**Scan WorkBench** is available for Teradyne’s J750™, FLEX™ and UltraFLEX™ families of testers. Improve debug efficiency on the systems you are already using with minimal training. By adding **Scan WorkBench** to your existing IG-XL environment, silicon debug time will be dramatically reduced – turning days of debug time into hours.

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[**www.teseda.com**](http://www.teseda.com)

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